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Design of Power Optimized circuit of LC Voltage Controlled Oscillator for use in GSM Handsets

A thesis submitted in partial fulfillment of the requirements for the degree of

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Electronics & Communication Engineering

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CERTIFICATE

This is to certify that the thesis titled "***Design of Power Optimized circuit of LC Voltage Controlled Oscillator for use in GSM Handsets"***, submitted to the National Institute of Technology, Rourkela by **Ms. Sohini Bandyopadhyay**, Roll No**. 108EC030** for the award of the degree of Bachelor of Technology in Electronics & Communication Engineering, is a bona fide record of research work carried out by her under my supervision and guidance.

The candidate has fulfilled all the prescribed requirements.

The thesis, which is based on candidate's own work, has not been submitted elsewhere for a degree/diploma.

In my opinion, the thesis is of standard required for the award of a Bachelor of Technology degree in Electronics & Communication Engineering.

To the best of my knowledge, she bears a good moral character and decent behavior.

Prof. D. P. Acharya

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Sohini Bandyopadhyay

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ABSTRACT:

The recent performance requirements for mobile phones have been extending its area of interest. Handsets need to have high resolution graphics, pictures, and applications. Consequently, the requirement for a longer battery life has become a bare necessity. This makes optimization of power a critical issue. Along with this cell phones need to be thin and have light weight.

A major portion of the power consumption of the handsets can be attributed to the LC oscillators used in the system. A Voltage Controlled Oscillator plays an important role in any communication system. It provides the frequency signal for down-conversion of input signals and also the carrier signals for the modulating signal.

Proper amplitude and low phase noise are two important criteria to achieve suitable performance for a VCO in any transceiver system. The strong combination of low phase noise specifications with very low power consumption (battery operation) forces designers to use LC-VCOs. A great research effort has been done in the design of integrated voltage controlled oscillators (VCOs) using integrated or external resonators, but as their power consumption still cannot be unacceptable, today's mobile phones commonly use external LC-VCO modules.

Inductors used in these oscillators are usually bulky and have high power consumption. The low power LC oscillator increases the standby time, thus improving the battery life. Extended battery life provides processing power at lower clock speeds, enabling low leakage process that optimizes power consumption and increases battery time. Also provides integrated and sophisticated systems with improved power management.

The main purpose of this project is to design a circuit for LC VCO to be used in GSM system with a tuning rage of 3-4GHz. Since the phase noise requirement for the system is less than 150dBc/Hz at 20 KHz offset. Also for a GSM system, the size of the inductor used in the oscillator is a major issue in determining its overall size, efforts will be made to optimize the size of the inductor as well.

Chapter

1

Introduction

1.1 Need of optimization of analog integrated circuits

With the rapid development and increasing demand of personal wireless communication, low cost and low power consumption are the most significant considerations for circuit design to enhance the battery lifetime and to improve the portability. Optimization is a more formal approach to simplification that is performed using a specific procedure or algorithm. Optimization requires a cost criterion to measure the simplicity of a circuit. As CMOS has been scaled down, it becomes an obvious choice to implement low-power integrated transceiver systems.

Among all blocks of the front-end except a power amplifier, the frequency synthesizer usually consumes most power. The problems of low power low phase noise VCO designs are the degradation of phase noise and low and non-constant output power by current exhaustion.

The IC design and manufacturing costs are increasing to the point that fewer products have the volume required to amortize the large upfront nonrecurring engineering costs. This is particularly the case for mixed-signal ICs that are designed in sub-100-nm technologies, where the technology advances are making application-specific system-on-chip designs technically feasible, but the economic realities require even higher product volumes. Design reuse and analog synthesis methodologies have substantially addressed the design cost and risk challenges. For a given circuit topology and specifications, simulation-based optimization and equation-based optimization have been effective for automating the design process. However, the large process parameter variability that is evident for nanoscale technologies along with the complex nature of parasitic coupling can cause the design risk, hence cost, to remain quite high, even for the best synthesis approaches.

For this reason, it is advantageous to design configurable analog/RF circuits that exploit circuit regularity. Importantly, such circuits can be precharacterized for the subtle device properties and coupling parasitics that are difficult to predict prior to layout and manufacturing. These regular

analog/RF circuits reduce the design risk and accommodate the tight time-to-market windows. While the design cost of configurable circuits exploiting regularity can be high, the cost is shared over multiple applications.

1.2 Different optimizations

More recently, circuit sizing has been cast as an optimization problem. As it is well known, casting any design problem into an optimization problem has two aspects:

Modeling the design problem as an optimization problem and solving the modeled problem. These steps are not independent and influence each other, for instance, the model of the problem will decide the optimization method that can be used. In the context of circuits, the accurate performance of circuits is that which is measured when the circuit is fabricated on silicon. Since the designer does not have access to this during the design process, the designer relies on a simulator which models the characteristics of the silicon elements and runs numerical algorithms to calculate circuit performance.

Name of Approach	Optimization Model	Optimization Algorithm
Simulation based Approach	SPICE evaluation Single objective, multiple constraints. Multiple objectives, multiple constraints.	Blackbox Optimization, e.g., Simulated Annealing, Stochastic Pattern search Multi-objective Genetic Algorithms.
Equation based Approach	Equation based evaluation Single objective, multiple constraints Multiple objectives, multiple constraints.	Blackbox Optimization, e.g., Simulated Annealing, Multi-objective Genetic Algorithms.
Geometric Programming	Posynomial equations with log-log transformation: Single objective, multiple constraints. Series of single objectives, multiple constraint problems	Convex optimization: Geometric Programming Reverse geometric programming.

Table 1- Types of optimization approaches

1.3 Convex Optimization

Geometric Programming and simulation-based approaches have both found acceptance in academia and industry, however the purpose and methodology to use them have been different. Here we compare them based on various metrics.

- Accuracy: In geometric programming, though the optimization method finds the global optima, inaccuracy creeps in due to the inaccuracy of the equations. There are two reasons for this inaccuracy. First, the derived equations use approximate circuit analysis. Second, the equations need to be in posynomial form and not all circuit equations can be modeled as posynomials. On the other hand, the optimization approach, i.e. geometric programming transforms the problem into a global optimization problem and guarantees global optima.

  In the case of simulation-based approaches, the modeling is accurate, since SPICE is used for performance evaluation. However the optimization method provides no guarantee of finding the global optima. The popularly used techniques of simulated annealing, evolutionary algorithms, etc. provide no mathematical guarantee of finding the actual optima and the optima within an error bound.

- Effort: The effort spent by the designer to use a tool based on the simulation based approach is moderate. The designer has to set up SPICE files for measuring different performance measures, select parameters to be optimized and set their ranges. The most time-consuming part here is that of setting the SPICE files. However, this effort can be reused across circuits with the same functionality.

  On the other hand, the effort spent in setting up a geometric program is much higher. The designer had to write equations for objectives and constraints themselves, which was cumbersome. Furthermore, the equations need to have posynomial form (in some recent commercial tools, this condition has been relaxed). This has to be done for each circuit topology. Though there has been some work in automatically deriving these equations, it hasn't yielded good results due to the inaccuracy and poor scalability of these approaches , the resultant expressions are not well-suited for optimization. No commercially available tool offers automatic modeling of equations to our best knowledge.

- Time: The time component for the circuit-sizing comprises of two durations. First, the time to setup the optimization problem. Second, the time taken by the optimization algorithm to size the circuit. In geometric programming, as discussed before, the time spent in setting the circuit optimization problem is high. The designer may take any amount of time to write the equations and usually must iterate because getting equations first time correct is not easy. Thus the time may include a debug cycle. Also, the time increases with the size and

complexity of the circuit. The second component of time, i.e. optimization time is low for geometric programming.

Metric	Geometric Programming	Simulation based Approaches
Accuracy	Inaccuracy in process and circuit modeling Accurate global optimization on given models	Accurate circuit models since SPICE is invoked in-loop Inaccuracy or no guarantee in stochastic optimization.
Effort	High designer effort in writing accurate equations	Little effort by designer needed for setting SPICE scripts for specification measurement and choosing variables to be optimized.
Time	High time in optimization problem formulation: Time spent in analyzing circuit and writing equations. Very fast optimization by interior-point methods	Little time needed in problem formulation High time of optimization because i. SPICE is invoked in loop of optimization, ii. Weak algorithm and not circuit specific
Suitability for system level Design	By generating fast trade-off curves for cells and their use for system-level optimization By combining cell-level equations to form system-level equations and optimizing the whole system.	Multi-objective approaches allow trade-off generation, which can be used for hierarchical bottom-up synthesis [9].
Suitability for robust optimization	Challenges in inclusion of robustness in a form optimizable by convex techniques Fast optimization on modeling	Challenges in decreasing number of SPICE simulations needed for robustness measurement.

Table-1 comparison of Geometric programming and simulation based approaches

Chapter

2

Convex Optimization

2.1 INTRODUCTION

Convex Optimization is a type of geometric program. A geometric program is a type of mathematical optimization problem characterized by objective and constraint function that have a special form. Recently developed solutions can solve even large scale GP problems extremely efficiently and reliably; and at the same time a number of practical problems, particularly in circuit theory, have been found to give similar results as to GPs. Getting these two together, we get effective solutions for the practical problems. The usual approach in GP modeling is to attempt to show a practical problem, such as an engineering analysis or designing problem, in the specified format. This formulation is usually exact; when this is not possible, settlement is done for an approximate formulation.

2.2 The GP modeling approach

A geometric program (GP) is a type of optimization problem characterized by objective and constraint functions designed in a special form. The importance of GPs comes from two relatively recent developments:

• New solution methods can solve even large-scale GPs extremely efficiently and reliably.
• A number of practical problems, especially in electrical circuit design have recently been found to be similar to (or well approximated by) GPs.

Putting these two issues in mind, we get effective solutions for the practical problems. Neither of these developments is widely known, at least not yet. Further improvements in GP solution methods will be developed, and, many more practical applications of GP will be discovered in the coming years. The general approach is to attempt to express a practical problem, such as an

engineering analysis or designing problem, in GP. In the best case, this formulation is an exact solution. When getting accurate results isn't possible, we settle for an approximate formulation. Formulating any practical problem as a GP is called GP modeling. On succeeding at GP modeling, we have an effective and reliable method for solving the practical problem.

We see that GP modeling is not just a matter of using some specific software package. It involves good knowledge about the subject, as well as creativity, to be done effectively. Moreover, success is never guaranteed: Many typical problems simply cannot be represented, or even approximated, as GPs. But when we succeed, the results are very useful and impressive, since we can reliably solve even larger issues with the practical problem. It is useful to compare GP modeling and modeling with general purpose non-linear optimization. NLP modeling is relatively easy, since the objective and constraint functions can be any nonlinear functions.

In contrast, GP modeling can be more difficult, since we are rather constrained in the form the objective and constraint function. Solving a GP can be very easy, but solving a general NLP is even more difficult, and always involves some compromise. When GP modeling is done, we are limiting the form of the objective and constraint functions. In exchange for accepting this limitation, though, we get the benefit of extremely efficient and reliable solution methods that solve large-scale problems efficiently.

A good analogy can be made with linear programming (LP). A linear program is an optimization problem which has an even constrained limitation on the form of the objective and constraint functions. Despite its restrictive form, LP modeling is widely used, in many practical fields, because LPs can be solved with great efficiency.

2.3Monomial and posynomial functions

Let $x_1, \ldots, x_n$ denotes n real positive variables, and $x = (x_1, \ldots, x_n)$ a vector with components x_i . A real valued function f of x, with the form

$$f(x) = cx_1^{a_1} x_2^{a_2} \cdots x_n^{a_n},$$

Where $c > 0$ and $a \in \mathbf{R}$, is called a monomial function, or more informally, a monomial of the variables $x_1, \ldots, x_n$. We refer to the constant c as the coefficient of the monomial, and we refer to the constants $a_1, \ldots, a_n$ as the exponents of the monomial.

Any positive constant is a monomial, as is any variable. Monomials are mostly closed under multiplication and division.

If f and g are both monomials then so are f*g and f/g. A monomial raised to any power is also a monomial:

$$f(x)^\gamma = (cx_1^{a_1}x_2^{a_2}\cdots x_n^{a_n})^\gamma = c^\gamma x_1^{\gamma a_1}x_2^{\gamma a_2}\cdots x_n^{\gamma a_n}.$$

The term 'monomial', as used here is similar to, but differs from the standard definition of 'monomial' used in algebra.

A sum of one or more monomials, i.e., a function of the form

$$f(x) = \sum_{k=1}^{K} c_k x_1^{a_{1k}} x_2^{a_{2k}} \cdots x_n^{a_{nk}},$$

Where $c_k > 0$, is called a *posynomial function* or, more simply, a *posynomial* (with K terms, in the variables $x_1, \ldots, x_n$). The term 'posynomial' is means to suggest a combination of 'positive' and 'polynomial'. Any monomial is also a posynomial. Posynomials are closed under addition, multiplication, and positive scaling. Posynomials can be divided by monomials (with the result also a posynomial): If f is a posynomial and g is a monomial, then f/g is a posynomial. If γ is a positive integer and f is a posynomial, then f^γ always makes sense and is a posynomial.

2.4Standard form geometric program

A vast number of design problems in engineering can be posed as constrained optimization problems, of the form:

minimize f0(x)
subject to fi(x) <= 0; i = 1…..m
hi(x) <= 0; i = 1…. p

Where x is a vector of decision variables, and the functions f0, fi and hi, respectively, are the cost, inequality constraints, and equality constraints.
As an example, consider the problem

$$\begin{aligned} \text{minimize} \quad & x^{-1}y^{-1/2}z^{-1} + 2.3xz + 4xyz \\ \text{subject to} \quad & (1/3)x^{-2}y^{-2} + (4/3)y^{1/2}z^{-1} \le 1, \\ & x + 2y + 3z \le 1, \\ & (1/2)xy = 1, \end{aligned}$$

with variables *x*, *y* and *z*. This is a GP in standard form, with $n = 3$ variables, $m = 2$ inequality constraints, and $p = 1$ equality constraints.

We can switch the sign of any of the exponents in any monomial term in the objective or constraint functions, and still have a GP. For example, we can change the objective in the example above to $x^{-1}y^{1/2}z^{-1} + 2.3xz^{-1} + 4xyz$ and the resulting problem is still a GP (since the objective is still a posynomial). But if the sign of any of the coefficients is changed, or change any of the additions to subtractions, the resulting problem is not a GP. If we replace the second inequality constraint with $x+2y-3z \leq 1$, then the resulting problem is not a GP (as the left-hand side is no longer a posynomial).

However, such problems can be very hard to solve in general, especially when the number of decision variables in x is large. There are several reasons for this difficulty:

[1] First, the problem "terrain" may be riddled with local optima.
[2] Second, it might be very hard to find a feasible point (*i.e.*, an x which satisfies all the equalities and inequalities), in fact the feasible set, which needn't even be fully connected, could be empty.
[3] Third, stopping criteria used in general optimization algorithms are often arbitrary.
[4] Forth, optimization algorithms might have very poor convergence rates.
[5] Fifth, numerical problems could cause the minimization algorithm to stop all together or wander.

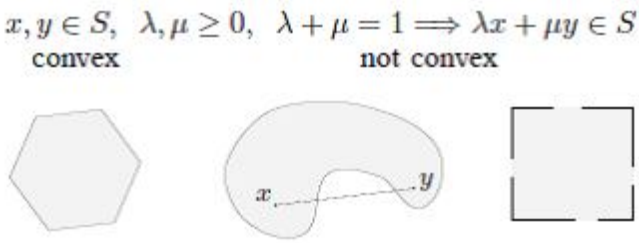
It has been known for a long time that if the fi are all convex, and the hi are affine, then the first three problems disappear: any local optimum is, in fact, a global optimum; feasibility of convex optimization
Problems can be determined unambiguously, at least in principle; and very precise stopping criteria are available using duality.

However, convergence rate and numerical sensitivity issues still remained a potential problem. If, in addition to convexity, the fi satisfied a property known as self-concordance, then issues of convergence and numerical sensitivity could be avoided using interior point methods. The self concordance property is satisfied by a very large set of important functions used in engineering. Hence, it is now possible to solve a large class of convex optimization problems in engineering with great efficiency.

A function f : **R**n ! **R**m is affine if it has the form linear plus constant f(x) = Ax + b.
Affine functions are sometimes loosely refered to as linear.

$$F(x) = A_0 + x_1A_1 + \cdots + x_nA_n$$

A set S € **R**n is a convex set if it contains the line segment joining any of its points.



Covex and non-convex sets Fig 1

A convex function should satisfy the following equation as well.

Where a, β are arbitrary constants.

2.5CVX Software

What is cvx?

cvx is a modeling system for convex programming. Disciplined Convex programs, or DCPs, are convex optimization problems that are described using a limited set of construction rules, which enables them to be analyzed and solved efficiently. cvx can solve standard problems such as linear programs (LPs), quadratic programs (QPs), second-order cone programs (SOCPs), and semidefinite programs (SDPs); but compared to directly using a solver for one or these types of problems, cvx can greatly simplify the task of specifying the problem. cvx can also solve much more complex convex optimization problems, including many involving nondifferentiable functions, such as `1 norms. You can use cvx to conveniently formulate and solve constrained norm minimization, entropy maximization, determinant maximization, and many other problems.

cvx is implemented in Matlab, turning Matlab into an optimization modeling language. Model specifications are constructed using common Matlab operations and functions, and standard Matlab code can be freely mixed with these specifications. This combination makes it simple to perform the calculations needed to form optimization problems, or to process the results obtained from their solution.

Chapter

3

LC Voltage Controlled Oscillator

3.1 INTRODUCTION

3.1.1 What is VCO?

A voltage controlled oscillator or as more commonly known, a vco, is an oscillator where the principal variable or tuning element is a varactor diode. The voltage controlled oscillator is tuned across its band by a "clean" dc voltage applied to the varactor diode to vary the net capacitance applied to the tuned circuit. A Voltage Controlled Oscillator (VCO) is an oscillating circuit whose output frequency changes in direct proportion to an input voltage. VCOs can be made to oscillate from a few Hertz to hundreds of GHz. Every wireless device in use today has some sort of voltage controlled oscillator inside it. For example, there is a least one VCO inside every cell phone that generates the Radio Frequency (RF) waves that are used to communicate by-directionally to the cell tower.

A VCO output frequency is stabilized or controlled with a Resonator. The lower the close-in Phase Noise requirement, the higher the Quality Factor (Q) of the Resonator needs to be. A Resonator can be as simple as an Inductor or as complex as a Quartz Crystal. The Table below lists some of the most popular Resonator types with their accompanying typical Q value in ascending order.

3.1.2 Types of VCO

VCOs can be generally categorized into two groups based on the type of waveform produced:

1) harmonic oscillators

2) relaxation oscillators.

Harmonic oscillators generate a sinusoidal waveform. They consist of an amplifier that provides adequate gain and a resonant circuit that feeds back signal to the input. Oscillation occurs at the resonant frequency where a positive gain arises around the loop. Some examples of harmonic oscillators are crystal oscillators and LC-tank oscillators. When part of the resonant circuit's capacitance is provided by a varactor diode, the voltage applied to that diode varies the frequency.

Relaxation oscillators can generate a sawtooth or triangular waveform. They are commonly used in monolithic integrated circuits (ICs). They can provide a wide range of operational frequencies with a minimal number of external components. Relaxation oscillator VCOs can have three topologies: 1) grounded-capacitor VCOs, 2) emitter-coupled VCOs, and 3) delay-based ring VCOs. The first two of these types operate similarly. The amount of time in each state depends on the time for a current to charge or discharge a capacitor. The delay-based ring VCO operates somewhat differently however. For this type, the gain stages are connected in a ring. The output frequency is then a function of the delay in each of stages.

Harmonic oscillator VCOs have these advantages over relaxation oscillators.

- Frequency stability with respect to temperature, noise, and power supply is much better for harmonic oscillator VCOs.
- They have good accuracy for frequency control since the frequency is controlled by a crystal or tank circuit.

A disadvantage of harmonic oscillator VCOs is that they cannot be easily implemented in monolithic ICs. Relaxation oscillator VCOs are better suited for this technology. Relaxation VCOs are also tunable over a wider range of frequencies.

3.1.3 Application of VCO

VCOs are used in:

- Function generators,
- The production of electronic music, to generate variable tones,

- Phase-locked loops,
- Frequency synthesizers used in communication equipment.

Voltage-to-Frequency converters are voltage-controlled oscillators, with a highly linear relation between applied voltage and frequency. They are used to convert a slow analog signal (such as from a temperature transducer) to a digital signal for transmission over a long distance, since the frequency will not drift or be affected by noise. VCOs may have sine and/or square wave outputs. Function generators are low-frequency oscillators which feature multiple waveforms, typically sine, square, and triangle waves. Monolithic function generators are voltage-controlled. Analog phase-locked loops typically contain VCOs. High-frequency VCOs are usually used in phase-locked loops for radio receivers. Phase noise is the most important specification for them. Low-frequency VCOs are used in analog music synthesizers. For these, sweep range, linearity, and distortion are often most important specs. Audio-frequency VCOs for use in musical contexts have largely been superseded by their digital counterparts, DCOs, due to their output stability in the face of temperature changes during operation.

3.2 COMPLEMENTARY CMOS LC VCO

Ring oscillator and LC oscillators are the two most commonly used circuit oscillators. Though the tuning range of ring oscillators is more than that of LC oscillator, due to the low phase noise requirements, LC oscillator are used in GSM systems. The LC tank oscillators in the circuit consist of a spiral inductor and moscap.

For this application, the LC-VCO represents the mainstream topology, due to its superior phase noise (PN) performance. The specifications are, center oscillation frequency *fc*, the tuning range, the PN, the power consumption, and the $K\text{vco} = fc/\partial V\text{tune}$.

In order to comply with the GSM-900 standard, the VCO has to cover the 3.3- to 4-GHz band, while driving a divider by 4, i.e., the tuning range is TR > 21%. The VCO has to provide a fine frequency control, with a target *K*vco between 50 to 100 MHz/V, which has to be kept under control over the 700-MHz coarse tuning.

The complementary cross-coupled VCO has two main advantages compared with NMOS transistors only cross-coupled topology. First, with the additional PMOS pair, the complementary topology offers higher transconductance to compensate for the loss of the tank

with less current consumption and hence is more power efficient. Second, matching the PMOS and NMOS transistors, the complementary topology provides better symmetry properties of the oscillating waveform, which decreases the up-conversion of 1/f noise of devices to the 1/f 3 phase noise region. Another advantage of using complementary topology without current sources is increment of voltage headroom. The lower output voltage swing level may lead to degrade phase noise performance.

3.3 Phase Noise Model of Leeson

A well known fact from oscillator theory, two conditions are required to make a feedback system oscillate:

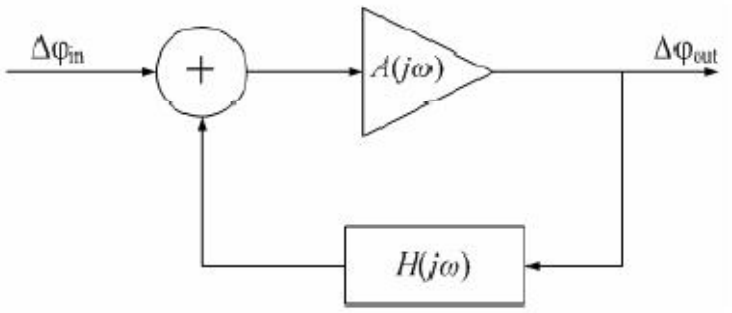
- The open loop gain must be greater than unity.
- Total phase shift must be 360 degrees at the frequency of oscillation.

An oscillator circuit can be a combination of an amplifier with gain A(jw) and a frequency dependent feedback loop H(jw)=BA. Oscillator has positive feedback loop at selected frequency.

- Frequency stability is a measure of the degrees of which an oscillator maintains the same value of frequency over a given time.
- Phase noise can be described as a short term random frequency fluctuation of signal. It is measured in the frequency domain and is expressed as a ratio of signal power to noise power measured in a 1Hz bandwidth at a given offset from the desired signal.
- Low oscillator phase noise is a necessity for many receiving and transmitter systems. Adjacent channel rejections as well as transmitter signal purity are dependent on the phase noise of the receiver local oscillator or transmit local oscillator.
- The local oscillator phase noise will limit the ultimate signal-to-noise ratio (SNR) which can be achieved when listening to a frequency modulated (FM) or phase modulated (PM) signal.
- The oscillator phase noise is transferred to the carrier to which the receiver is tuned and is then demodulated by the FM discriminator. The phase noise results in a constant noise power output from the discriminator.
- Local oscillator phase noise will affect the bit error rate (BER) performance of a phase-shift keyed (PSK) digital transmission system. A transmission error will occur any time if the local oscillator phase, due to its noise becomes sufficiently large that the digital phase detection makes an incorrect decision as to the transmission phase.

Leeson's is one of the most famous models for predicting the phase noise in a feedback oscillator. But there are several limitations and drawbacks to this model. Leeson's equation involves some key parameters, and these parameters are often determined by the oscillator structure and the oscillator circuit itself. Then a directly application of the Leeson's model without care would lead to erroneous results. Leeson's also assumed that the amplifier gain is remained a constant versus the frequency close the carrier frequency; and the filter transfer function is considered symmetrical on both sides of the carrier frequency. For a state of the art crystal oscillator the flat noise floor should be about -180dBc/Hz. The Leeson equation does not obviously describe these oscillators well, and the flat noise floor is about 15dB lower than that would be expected from the Leeson model.

Leeson took oscillators as linear time invariant feedback systems. A mathematical analysis of this " heuristic " model has been proposed. The oscillator can be seen as an amplifier which has feed-back through a filter. If the gain is sufficient to overcome the filter attenuation and the phase shift is correct, then oscillations will occur. If the amplitude of the oscillation is limited somehow, the amplifier can be made to operate in linear class A mode and then the Leeson's model will describe the main characteristics of the sideband noise.



Leeson's phase noise model of feedback oscillator—fig 2

Leeson [5], using a single resonator feedback network, has derived the following expression that we called Leeson formula:

$$PN = 10\,log_{10}\left\{\frac{2kTF}{P_s}\left[1+\left(\frac{f_c}{2Q\Delta f}\right)^2\right]\left[1+\frac{\Delta f_1/f^3}{\Delta f}\right]\right\}$$

Where *k* is the Boltzmann constant, *T* is the temperature, *F* is the excess noise factor, *Ps* is the signal power, *Q* is the tank quality factor, and $\Delta f1/f3$ is the corner frequency. The PN can be thus optimized by maximization of *Q* or *Ps*.

From the phase noise model of Leeson some conclusions can be drawn as follows:

(1) Phase noise (at a given offset frequency) improves with both the carrier power and Q_L increasing. These dependencies make sense. Increasing the signal power improves the ratio simply because the thermal noise is fixed, while increasing Q_L improves the ratio because the tank ' s impedance falls off as $1/(2\ Q_L f_m)$.

(2) At large frequency separations only the first line becomes non-zero. It says that the flat noise floor in dBc/Hz simply is the difference between the power delivered into the amplifier and the noise floor of the amplifier in dBm/Hz. Let ' s suppose a low noise figure like 5 dB and a very high power level into the amplifier like 3dBm one finds that the flat noise floor is expected no more than -174dBc/Hz.

(3) Close to the carrier, the bandwidth of the filter causes the noise that is produced at the amplifier output to be amplified with a positive feedback that depends on the frequency separation. The gain increases by 20dB/decade.

(4) At some frequency separation flicker noise will cause phase modulation. To some extent, the transistor amplifier is a phase modulator and the current variations through the transistor will change the phase shift through the amplifier very slightly. The flicker noise slopes at 10dB/decade and changes the slope from 20dB/decade to 30dB.

At first a simple LC VCO circuit is employed and its optimized power is obtained. The figure below shows the circuit diagram. The circuit consists of two cross-coupled nmos transistors in parallel with an inductor and two moscaps in series. A tail current supplies constant current to the transistors.

3.4 General Oscillator Circuit:

Design Constraints

To design the oscillator we specify the following variables:

- **Spiral inductor:** number of turns n, turn width w, turn spacing s and outer diameter dout. Transistors: width (Wn and Wp) and length (Ln and Lp).
- **Varactor:** maximum value Cv;max and minimum value Cv;min.
- **Load capacitance:** Cload.
- **Bias current:** Ibias. Since the thermal noise of the tail current source in the vicinity of the frequency of oscillation does not affect the phase noise of the oscillator due to its differential operation, we use Ibias as a design parameter rather than the bias transistor dimensions.

Model for the LC Oscillator:

Inductor Model:

A spiral inductor is characterized by the number of turns n, the turn width w, the turn spacing s, and the outer diameter dout. The inductance L can be modeled by a monomial function of the design variables.

Varactor Model:

There are several varactor options for frequency tuning such as junction diodes, MOS capacitors and accumulation mode capacitors. In this project we use a moscap with a constant capacitance for providing the variable capacitance.
This 90 nm digital CMOS process has no analog extensions, so only two types of capacitors are available for a varactor implementation: a metal flux (MFLUX) capacitor and a MOS capacitor. Although the intrinsic of a MFLUX capacitor is reasonably high, the effective varactor (with the switches included) in a high-capacitive state is less than 20 at 3.6 GHz. Since it is desired to have a high frequency step size for the PVT bank, which requires large MFLUX capacitor dimensions, large switches would keep the effective high but, due to their parasitic effects, the ratio would also decrease. MOS capacitor has the advantage of having a significant smaller process variation than that for a MFLUX capacitor. Because there are no series switches connected to the capacitor to control the state of the MOS varactor, the capacitance has a high quality factor.

Transistor Model:

Transconductance:

A simple model for the transconductance is given as:

$$g_{\mathrm{m}} = \mu C_{\mathrm{ox}} W E_{\mathrm{sat}}/2,$$

Output Conductance:

$$g_{\mathrm{d}} = \lambda I^{0.6} L^{-1} W^{0.4},$$

Tank Model values:

- ***Tank inductance:***

$$L_{\mathrm{tank}} = 2L.$$

- ***Tank capacitance:***

$$C_{\mathrm{tank}} = \begin{array}{l} \frac{1}{2}(4C_{\mathrm{gd,n}} + C_{\mathrm{gs,n}} + C_{\mathrm{db,n}} + 4C_{\mathrm{gd,p}} \\ +C_{\mathrm{gs,p}} + C_{\mathrm{db,p}} + C_L + C_v), \end{array}$$

- ***Tank load conductance:***

$$g_{\mathrm{tank}} = (g_{\mathrm{d,n}} + g_{\mathrm{d,p}} + g_v + g_L)/2,$$

Where the values of the parameters are calculated as follows:

$$g_v = \frac{C_{\mathrm{var}}\omega}{Q_v}, \qquad g_L = \frac{1}{R_{\mathrm{p}}} + \frac{1}{(L\omega)^2 / R_{\mathrm{s}}}.$$

Where gv is effective varactor conductance and gl is effective parallel conductance

Chapter

4

Results & Discussions

4.1 Phase noise Vs Power graph obtained from MATLAB simulation

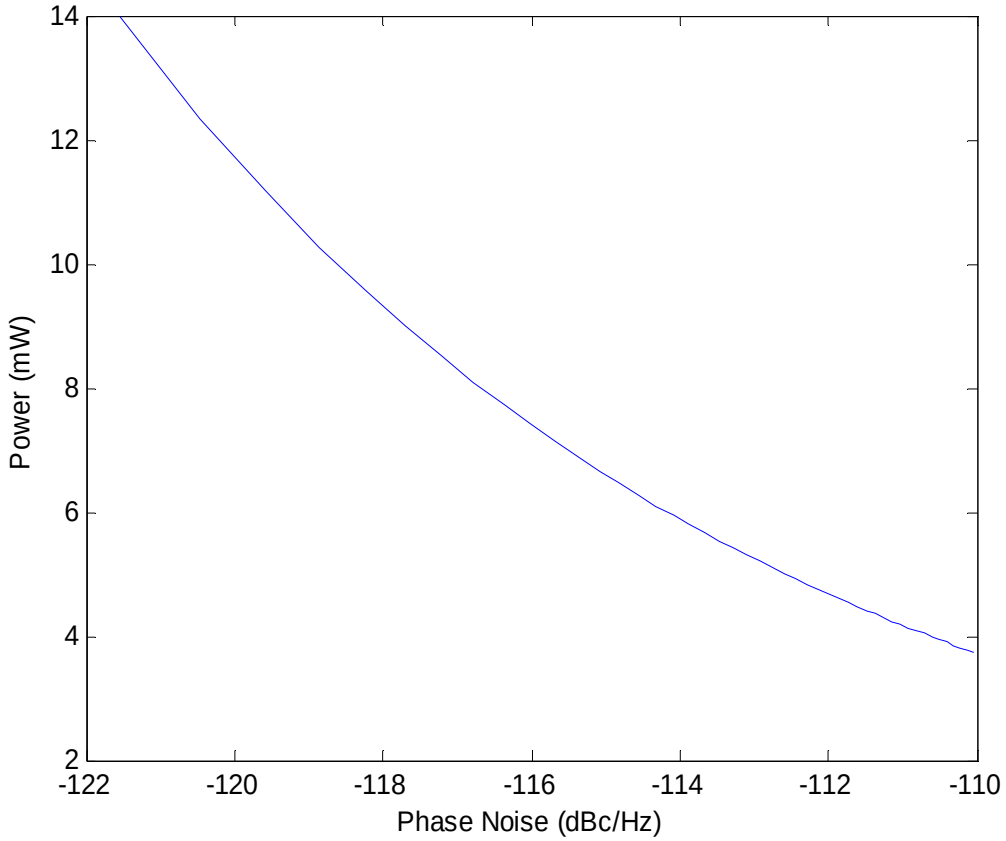


Fig 3

This output curve shows a tradeoff between the power and phase noise parameter of the circuit. As the phase noise increases, the power gradually decreases.

4.2 General Oscillator Circuit:

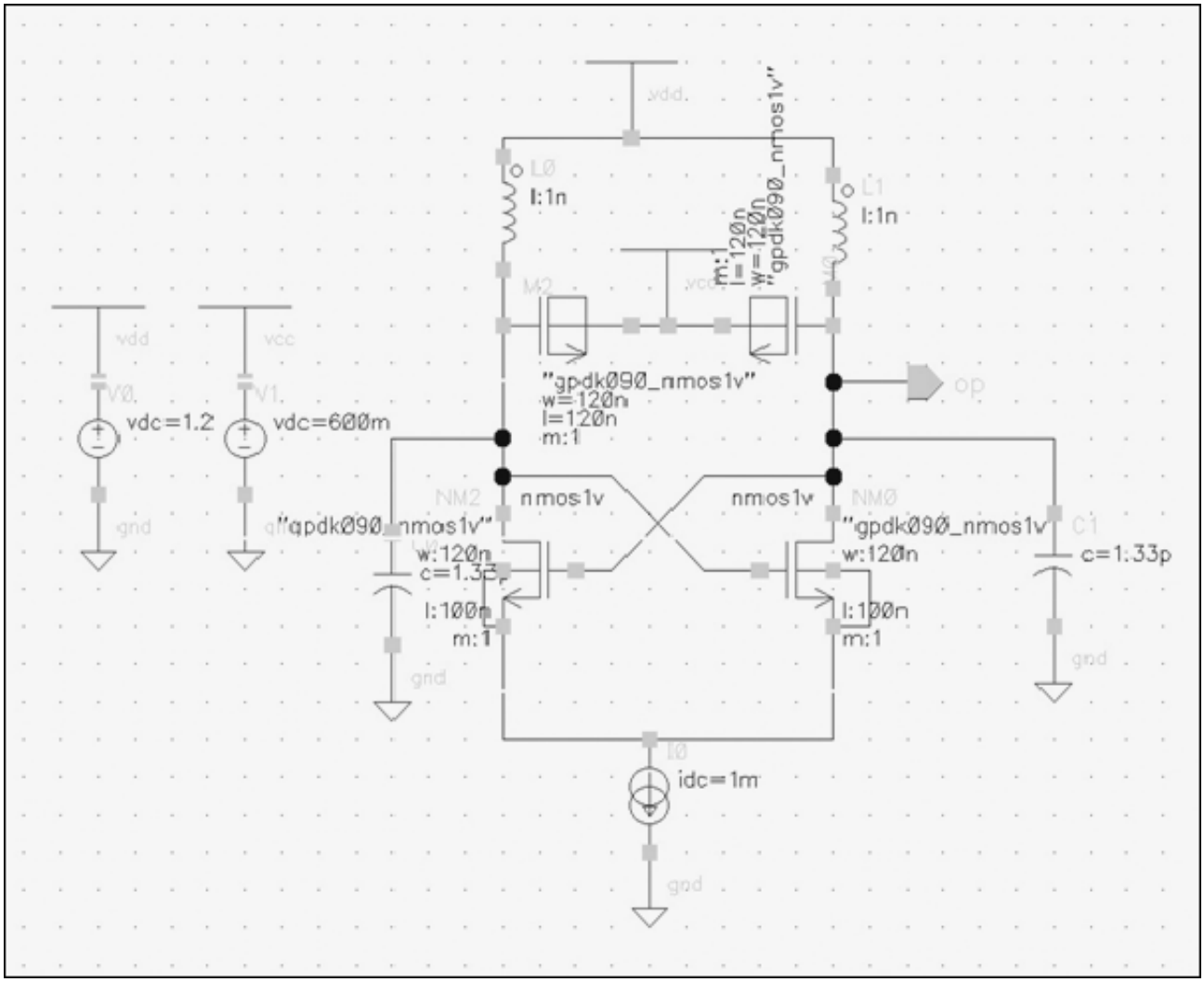


FIG 4

4.3 Parameter values obtained from convex optimization code

Parameter	Value
Vdd	2.5 V
Ltail	1nH
Lcoil	12.9nH
Cmoscap	690fF

Table 3

Oscillations obtained from transient analysis of the circuit:

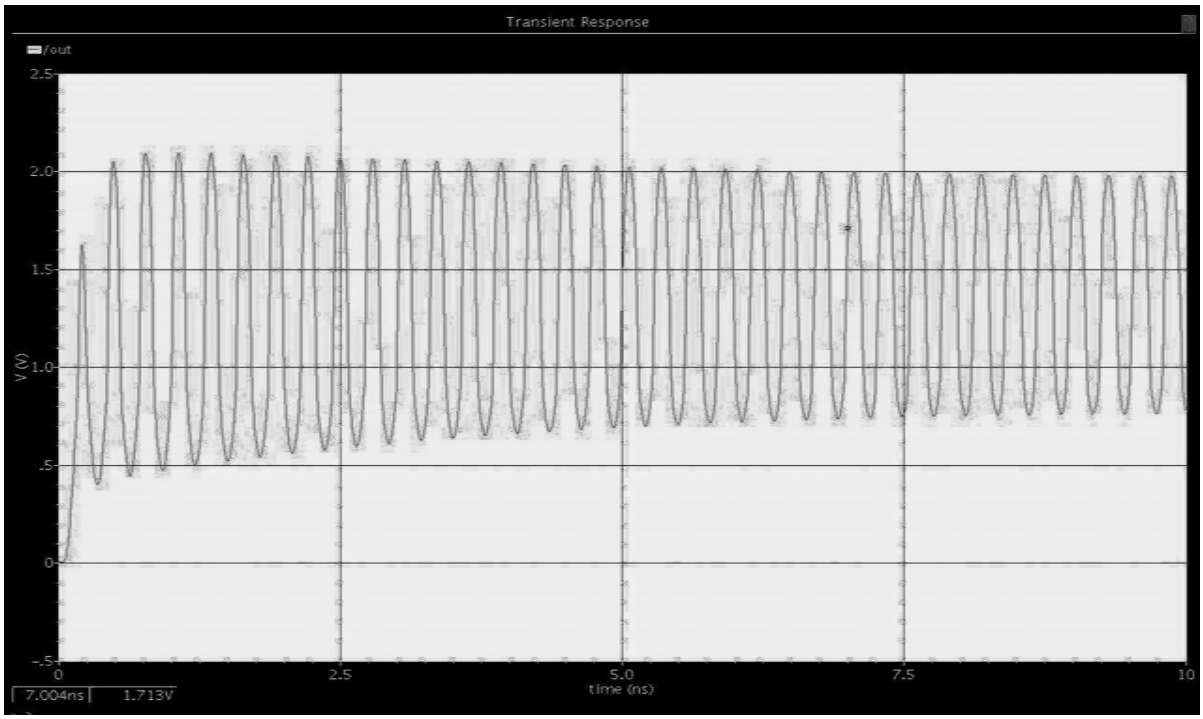


FIG 5

The output frequency of the simulation is 3.88 GHz.

The power analysis of the circuit of fig-4

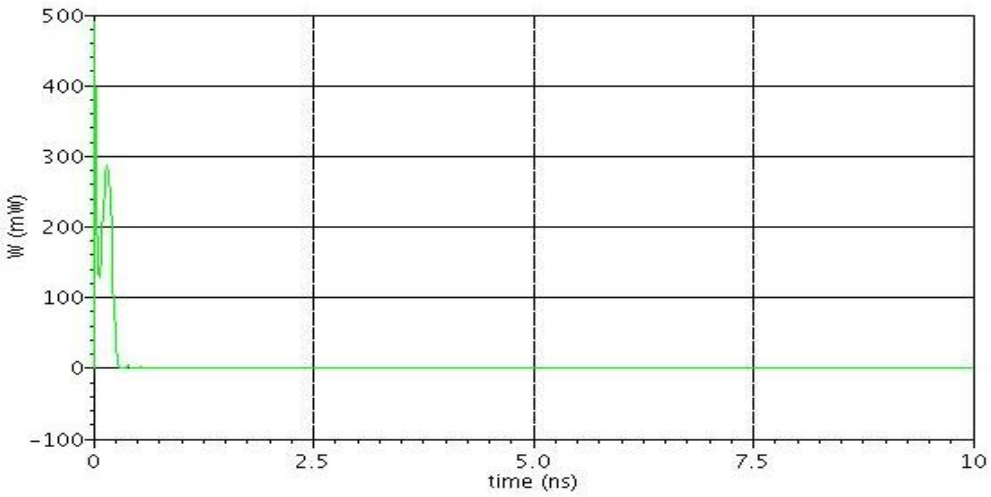


Fig 6

The average power of the circuit is 5.37mW.

The phase noise analysis of the circuit in fig-4:

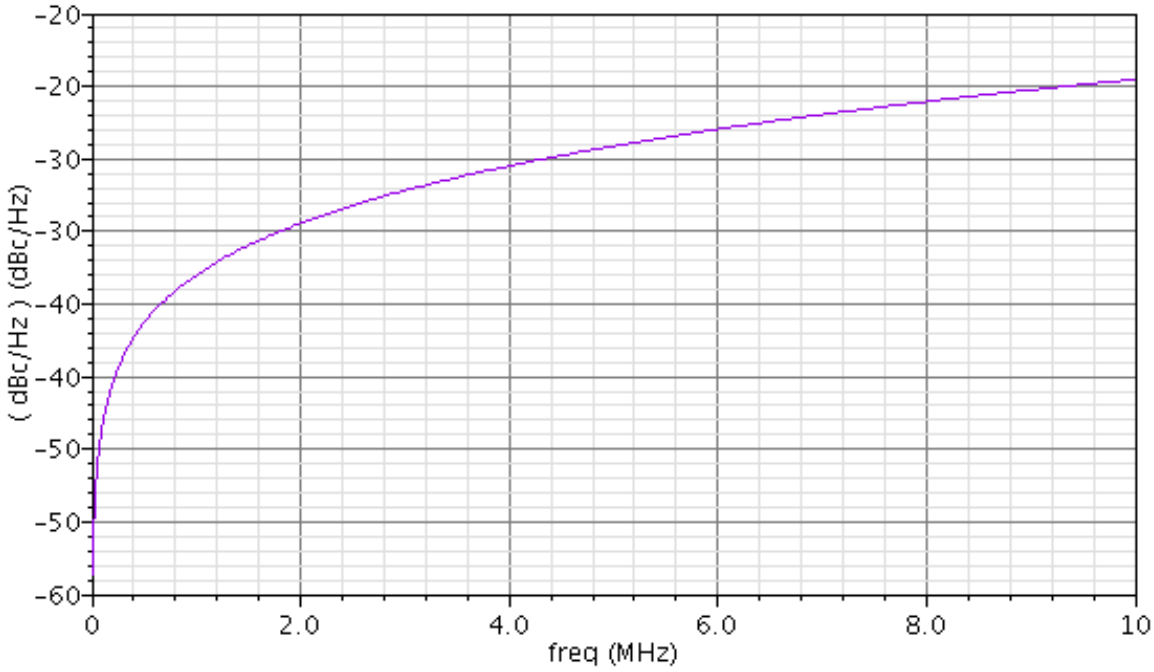


FIG 7

The average phase noise of the circuit is -78 dBc/Hz

4.4 VCO TOPOLOGY for GSM circuit

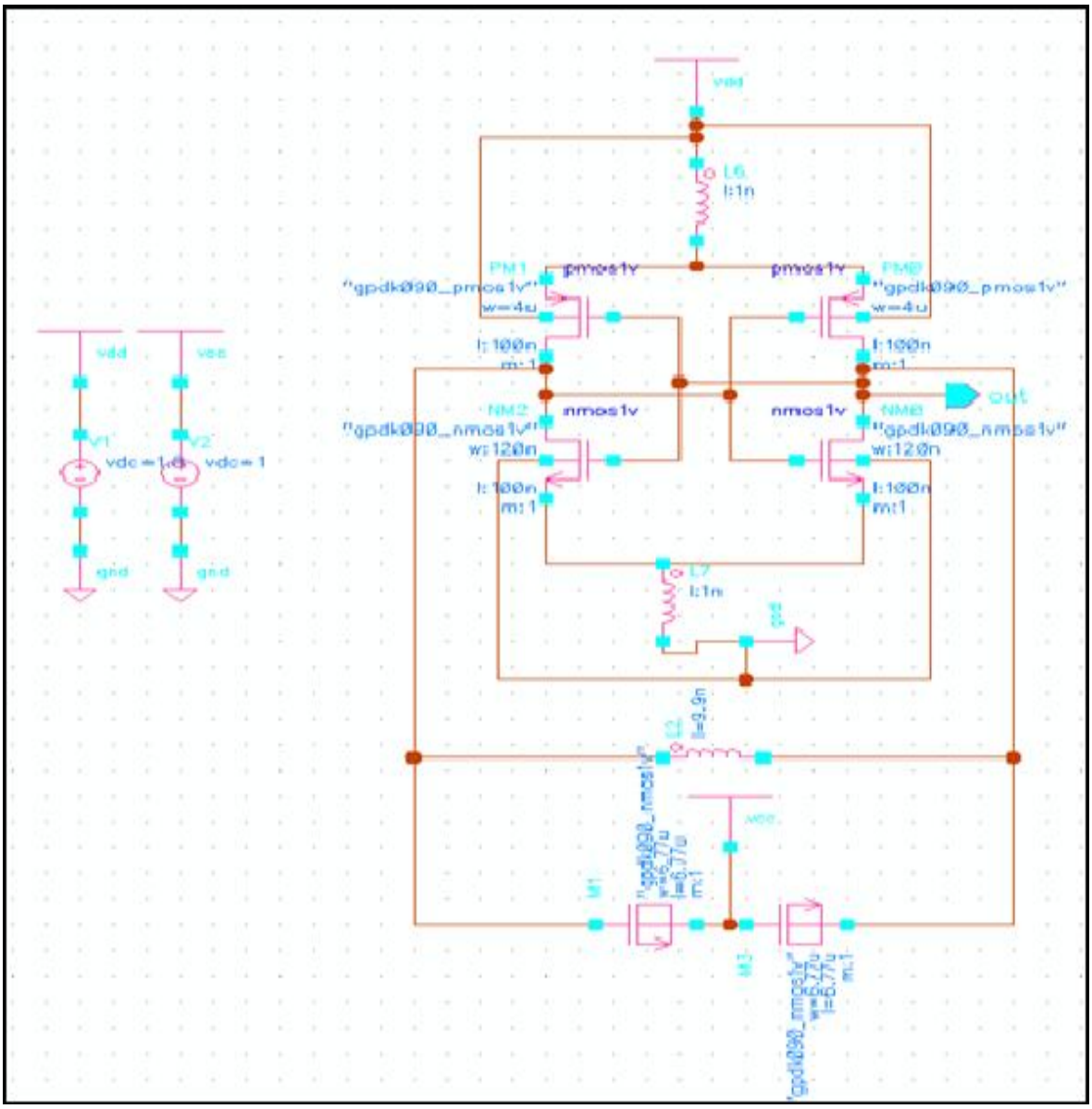


FIG 8

4.5 Parameter values obtained from convex optimization code

Parameter values	Convex Optimization
Ltail	0.9nH
Lcoil	12.9nH
Cmoscap	690fF
Freq	3.77GHz
Power	0.3688mW
Phase Noise	-110dBc/Hz

Table 4

In the circuit, the active bridge has both nMOS and pMOS cross-coupled pairs. This optimizes the current consumption for a given negative resistance and ensures better reliability with respect to only nMOS or pMOS topologies. Here no current mirror is present, thus removing a substantial noise source at the cost of absence in control on the current consumption. Two tail coils (Ltail) connect the tail nodes to the power supply and ground, preventing large signal distortion by the active bridge and mitigating its impact on the quality factor Q of the LC-tank. The larger the frequency, the more effective the coils are, provided that the self-resonance frequency is larger than the oscillating frequency of the tail node.

Since the VCO topology sketched in Fig 7. Maximizes the output swing (i.e., Ps), we start the design sizing the coil Lcoil with the aim of maximizing its quality factor QL ≈ Q. The maximization of QL is achieved by maximizing the Lcoil/Rs ratio (where Rs is the series resistance of the coil) within a given area constraint. This is achieved by optimizing the coil layout: Increasing the number of windings improves Lcoil and reduces Rs; an upper limit to the number of windings is given by the increase in the parasitic capacitance between the windings.

4.6 Key features of the given circuit:

The above selection of the structure mainly fulfills the following considerations:

1) **Good driving capability.** No-tail current source bias makes the oscillator work in the voltage restricted areas, so the output amplitude of oscillator can be infinitely close to the supply voltage. Therefore, it is more robust than that with current bias.

2) **Lower phase noise.** The flicker noise of tail current source as well as the noise at even harmonics mixing up near the fundamental frequency deteriorates the phase noise of VCO in the low frequency. But no-tail current source structure can avoid this problem.

3) **Smaller chip area.** In case of current source bias, it needs an inductance at the tail current source resonating with the parasitic capacitance at $2\omega 0$ frequency to form high impedance in order to reduce flicker noise of tail current source and the noise at even harmonics. This additional inductance occupies large chip area.

4) **High stability.** The change of the current of tail current source with technology and temperature is larger than that of intrinsic current. But the structure of no-tail current source reduces the output impedance of the differential common mode point, increases the return loss and reduces the *Q* value of resonant loop.

The LC oscillator was designed to achieve minimal dynamic power consumption for a certain frequency. The optimization has the form:

minimize: Power(Vdd * I)
subject to: $PN(I, gt_{ank}, C_{tank}, L, Vsw) < PN_{max}$
$f_{resonant}(C_{tank}, L) = fo$
$LG_{min} \leq$ Loop gain(I, g_{tank})
$Vsw \leq V_{dd}$
$Vsw \leq \frac{I_{bias}}{g_{tank}}$

where fo is the given resonant center frequency, PNmax is the maximum phase noise specification, LGmin is the minimum loop gain specification and Vdd is the power supply voltage. Simulation of the matlab code using the above analysis gives the values for Ltail and Lcoil with the phase noise to frequency curve as shown in fig 3.

Oscillations Obtained by transient analysis of circuit:

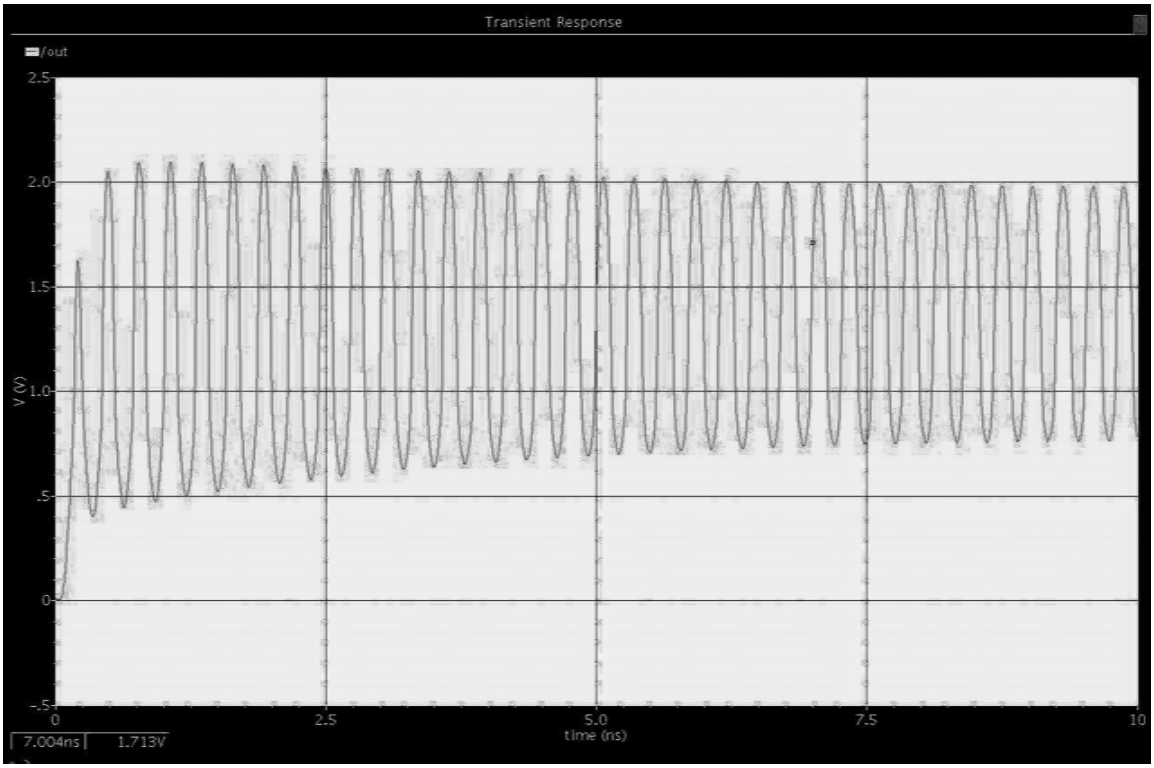
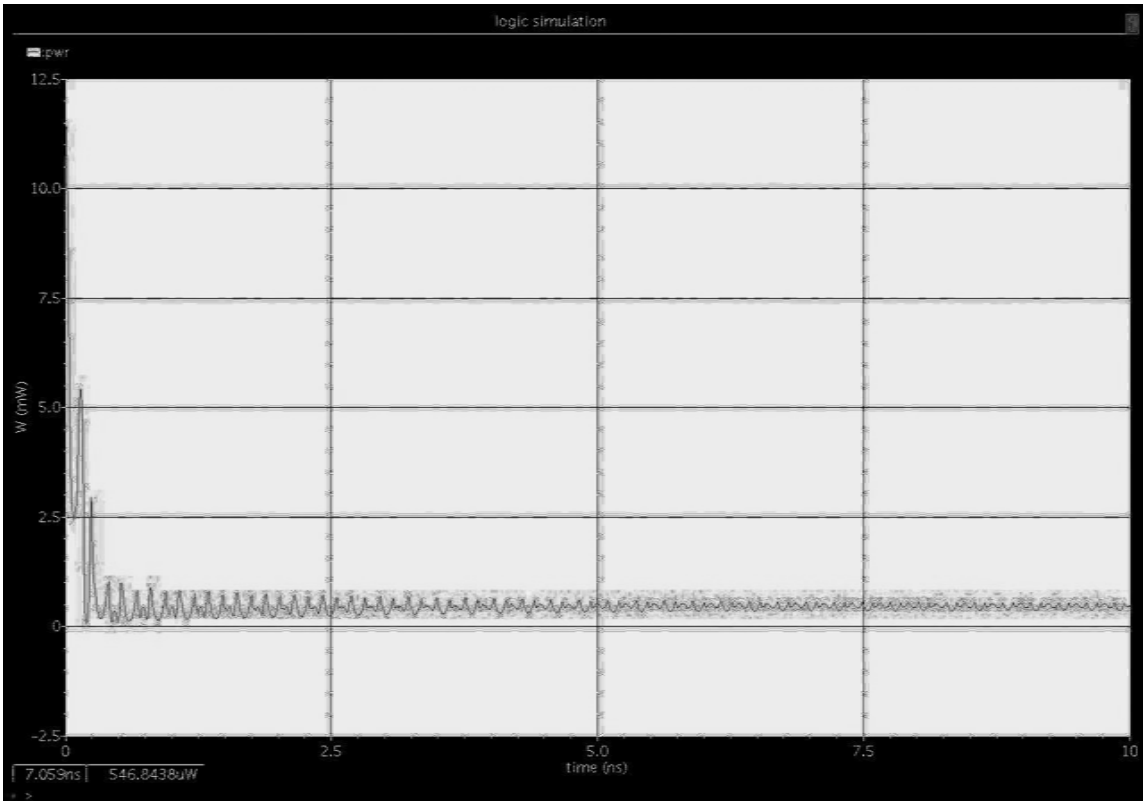


FIG 9

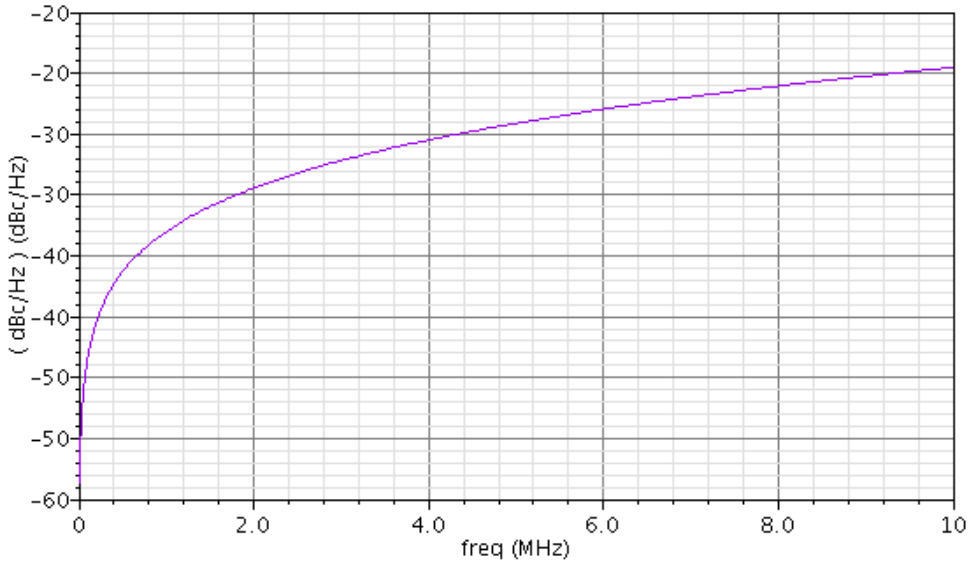
The frequency of the given output simulation is 3.87GHz.

The power analysis of the circuit in fig-7:



The average power of the given circuit is around 5.19mW.

The phase noise analysis of the circuit in fig-7:



the average phase noise value of the given circuit simulation is -117 dBc/Hz.

Discussions

Comparison of values for general oscillator circuit:

Power value from original circuit	Power value from the optimized circuit
12.5mW	5.37mW

Phase noise value from original circuit	Phase noise value from optimized circuit
-100 dBc/Hz	-87 dBc/Hz

Comparison of values for GSM oscillator circuit:

Power value from original circuit	Power value from the optimized circuit
12.7mW	5.19mW

Phase noise value from original circuit	Phase noise value from optimized circuit
-141 dBc/Hz	-117 dBc/Hz

Chapter

5

Conclusion

- Using the parameter values from the convex optimization code, the power consumption of both the circuits reduced drastically.
- As the power reduces the phase noise of the resulting circuit increases relatively.
- Thus there has to be an optimum tradeoff between the two parameters.
- There exists a tradeoff between the PMOS transistor width and the stabilizing time for the output.
- This same technique can be used for other applications involving oscillator circuits and optimal results can be obtained.

Chapter

6

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Code for optimization of LC oscillator circuit (with tradeoff curve):

The problem data given is as follows:

```
Vdd   = 5       % voltage
CL    = 1.33e-12    % load capcitance
F     = 3.5e9       % operating frequency in Hz
omega = 2*pi*F      % operating freq. in radians

FOff    = 6e5       % offset frequency for phase noise calculation
LoopGainSpec = 2.0  % loop gain spec
Vbias  = 0.2        % non-ideality of current mirror

% tuning specifications

T         = 0.1     % +/- tuning range as a normalized value
CvarRatio = 3       % maximum to minimum value of CVar
CswBits   = 3
CswSegs   = 2^(CswBits)
CvarCswLSBOverlap = 2
```

The phase noise parameter for the tradeoff curve is varied from the range :

```
PNSpec=0.7e-12:0.2e-12:1e-11
```

The optimization variables that are taken into account are

```
variable D        % diameter of loop inductor
variable W        % width of loop inductor
variable SRF      % self resonance frequency
variable l        % length of CMOS transistor
variable w        % width of CMOS transistor
variable I        % maximum current through CMOS transistor
variableVOsc% differential voltage amplitude
variable CT       % total capacitance of oscillator
```

variableCsw% *maximum switching capacitance*
variableCvar% *minimum variable capacitance*
variableIBias% *bias current*
variableCMaxFreq% *capacitor max frequency*

The main objective is to minimize power of the circuit minimize power i.e.,

minimize(Vdd*IBias)

Subject to the constraints:

*%*****%*

% loop inductor definitions and constraints %

*%*****%*

SRFSpec = 3*F
omegaSRF = 2*pi*SRF

% inductance[3]
L = 2.1e-06*D^(1.28)*(W)^(-0.25)*(F)^(-0.01)
% series resistance
R = 0.1*D/W+3e-6*D*W^(-0.84)*F^(0.5)+5e-9*D*W^(-0.76)*F^(0.75)+0.02*D*W*F
% effective capacitance
C = 1e-11*D+5e-6*D*W

% area, tank conductance, and inverse quality factor
Area = (D+W)^2
G = R/(omega*L)^2
invQ = R/(omega*L)

% loop constraints
Area <= 0.25e-6
W <= 30e-6
5e-6 <= W
10*W <= D
D <= 100*W
SRFSpec<= SRF
omegaSRF^2*L*C <= 1

*%*****%*

```
    % transistor definitions and constraints %
    %****************************************%
GM  = 6e-3*(w/l)^0.6*(I/2)^(0.4)
GD  = 4e-10*(w/l)^0.4*(I/2)^(0.6)*1/l
Vgs = 0.34+1e-8/l+800*(I*l/(2*w))^0.7
Cgs = 1e-2*w*l
Cgd = 1e-9*w
Cdb = 1e-9*w

% transistor constraints
    90e-9 <= w
    100e-9 <= l
    l <= 1e-6

    %****************************************************%
    % overall LC oscillator definitions and constraints %
    %****************************************************%
invVOsc = (G+GD)/IBias

    % phase noise
kT4  = 4*1.38e-23*300
    kT4G = 2*kT4
LoopCurrentNoise = kT4*G
TransistorCurrentNoise = 0.5*kT4G*GM
    PN = 1/(160*(FOff*VOsc*CT)^2)*(LoopCurrentNoise+TransistorCurrentNoise)

% capacitance
Cfix = C+0.5*(CL+Cgs+Cdb+4*Cgd) % fixed capacitance
CDiffMaxFreq = Cfix+0.5*Cvar

invLoopGain = (G+0.5*GD)/(0.5*GM)

    % LC oscillator constraints
    PN <= PNSpec
omega^2*L*CT == 1
omega^2*(1+T)^2*L*CMaxFreq == 1
    4*T/((1-T^2)^2)*CT <= Csw*(1+CvarCswLSBOverlap/CswSegs)
```

```
Csw*CvarCswLSBOverlap/CswSegs<= 0.5*Cvar*(CvarRatio-1)
CDiffMaxFreq<= CMaxFreq
    VOsc+2*Vbias<= 2*Vdd
VOsc*invVOsc<= 1
invLoopGain*LoopGainSpec<= 1 % loop gain spec
Vbias+Vgs+IBias/2*R/2 <= Vdd% bias constraint spec
    I == IBias
```